CASCADE DRIVING CIRCUIT FOR LIQUID CRYSTAL DISPLAY

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application No. 92129090, filed on October 21, 2003.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention generally relates to a driving circuit for a liquid crystal display, and more particularly to a cascade driving circuit.

Description of Related Art

[0002] The driving circuit for a liquid crystal display (LCD) in conventional scheme is primarily categorized into a parallel driving circuit and a cascade driving circuit. A parallel driving circuit transmits a data signal to a designated [[a]] driving circuit unit via a bus, thus it takes a substantially large layout and routing area on a printed circuit board.

[0003] Referring to FIG. 1, a parallel driving circuit structure is illustrated herein. The data signal 122 of the LCD 110 in the figure is supplied by a plurality of driving circuit units 120, which are manufactured with Tape Carrier Package (TCP) technology. The driving circuit units 120 supplies primitive data signal 144 via a data bus 142, and the data signal 144 is transmitted to a designated driving circuit unit 120 via the data bus 142 controlled by a timing controller 140. The foregoing data bus 142 and the

timing controller 140 are both disposed on a printed circuit board 130. Since bus structure and timing controller are included, the significant layout and routing area on the printed circuit board 130 are required. Therefore, a cascade style driving circuit was developed for pursuing miniaturization in electronic products.

[0004] A cascade driving circuit is formed from connecting ~~ed from~~ a plurality of driving circuit units. The type of circuit transmits the data signal to a designated driving circuit unit stage by stage.

[0005] Referring to FIG. 2, a cascade driving circuit structure is described herein. The data signal 222 for the LCD 210 in the figure is supplied by a plurality of driving circuit units 220, which is formed via Chip On Glass (COG) technology on an LCD substrate 210. The timing controller 240, being disposed on the PCB 230, generates the cascade signal 224 and transmits the cascade data signal 224 to a designated driving unit 220 stage by stage via the cascade structure of the driving circuit units 220. The transmitting channel of the cascade signal 224 is formed on the LCD substrate 210 with Wire On Array (WOA) technology.

[0006] Referring to FIG. 3, FIG. 3 illustrates a attenuation characteristic that[[of]] the cascade signal 310 is transmitted via WOA wire 320 to obtain another cascade signal 330 ~~via WOA wire 320 is illustrated as a signal attenuation diagram herein~~.

[0007] Since the cascade driving circuit is disposed on an LCD substrate and WOA technology is applied to connecting wires between each of the driving circuit units, the large impedance is inevitable, as well as the signal attenuation and major power consumption.

SUMMARY OF THE INVENTION

[0008] An object of the present invention is to provide a driving circuit for an LCD, so as to reduce the power consumption of the conventional cascade driving circuit.

[0009] Another object of the present invention is to provide a driving circuit for an LCD, so as to reduce ~~improve~~ the signal attenuation of the conventional cascade driving circuit.

[0010] A differential signal interface circuit is provided in this present invention, for disposing between cascade driving circuit units for reducing the power consumption.

[0011] Another signal amplifier is provided in this present invention, so as to reduce the signal attenuation.

[0012] A cascade LCD driving circuit is provide in this present invention, including a plurality of driving circuit units, a plurality of differential signal transmitters, and a plurality of differential signal receivers. The driving circuit units are connected in a cascade connection~~fashion~~, and a data signal is generated for driving the LCD. One of the differential signal transmitters is disposed [[to]]in each of the driving circuit units, so as to generate differential signals for driving a next stage of the driving circuit unit. One of the differential signal receivers is disposed in ~~with~~ each of the driving circuit units, so as to receive a differential signal from the previous stage of the driving circuit unit.

[0013] In one preferred embodiment of the present invention, the foregoing differential signal transmitter further includes a signal amplifier, which converts and amplifies the differential signal before transmitting the differential signal from the differential transmitter.

[0014] Since a differential signal interface circuit is disposed between the driving circuit units, the differential signal interface circuit includes a differential signal transmitter being disposed in the timing controller, and a differential signal transmitter and a receiver being disposed in each of the driving circuit units. Since the differential signal transmits signals with differentiating a positive signal and its inverse negative signal, voltage is lowered as well as power consumption is reduced comparing to the conventional transmission method via the voltage variation.

[0015] According to another preferred embodiment of the present invention, since the primitive differential signal is partially amplified after conversion, signal attenuation is compensated in advance during transmission, where a signal amplifier is disposed [[with]]in the differential signal transmitter among each of the driving circuit unit and the timing controller.

[0016] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 is a structure diagram illustrating a parallel driving circuit according to a conventional scheme.

[0018] FIG. 2 is a structure diagram illustrating a cascade driving circuit according to a conventional scheme.

[0019] FIG. 3 is a waveform diagram illustrating the signal attenuation as data transmitted according to a conventional scheme.

[0020] FIG. 4 is a block diagram illustrating a driving circuit unit according to one preferred embodiment of the present invention.

[0021] FIG. 5 is circuit diagram illustrating a differential signal interface circuit according to one preferred embodiment of the present invention.

[0022] FIG. 6 is a block diagram illustrating a driving circuit unit including signal amplifier according to one preferred embodiment of the present invention.

[0023] FIG. 7 is a waveform diagram illustrating signal amplification according to one preferred embodiment of the present invention.

[0024] FIG. 8 is a circuit diagram illustrating the signal amplifier according to one preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] Referring to FIG. 4, it is a block diagram illustrating a driving circuit unit according to one preferred embodiment of the present invention. A differential signal 412 is transmitted from a previous stage to a present stage, and is read [[to]]by a driving circuit unit 410 via a differential signal receiver 420, and the driving circuit unit 410 generates[[ing]] a differential signal 414 which is transmitted to a next stage thereafter via a differential signal transmitter 430.

[0026] The aforementioned differential signal transmitter 430 and the receiver 420 are illustrated as shown in FIG. 5. In the figure, the drains of the transistor 520 and transistor 530 are coupled to the current source 510, the source of the transistor 520 is coupled to the drain of the transistor 540 where an output signal 522 is drawn, the source of the transistor 530 is coupled to the drain of the transistor 550 where an output signal 532 is drawn, and the sources of the transistor 540 and of the transistor 550 are

coupled to the ground voltage. The signal 522 and the signal 532 [[make]]form the differential signal that is transmitted by the differential transmitter 501. The differential signal receiver 502 makes ~~couples~~ the signal 522 coupled to a first end of the resistor 570 and the negative terminal of the amplifier 560, and makes ~~couples~~ the signal 532 coupled to a second end of the resistor 570 and the positive terminal of the amplifier 560.

[0027] Another preferred embodiment is provided in this present invention for eliminating the signal attenuation during conventional differential signal transmission. Referring to FIG. 6, it is a block diagram illustrating a driving circuit unit including a signal amplifier. A differential signal 512 is propagated from a previous stage to this present stage, and is read [[to]]by the driving circuit unit 610 via the differential signal receiver 620. Thereafter, the differential signal transmitter 630 generates a differential signal, which is converted and partially amplified by the signal amplifier 640, and a differential signal 614 is obtained and transmitted to a next stage thereby.

[0028] Referring to FIG. 7, it is a waveform diagram of signals that are amplified by the amplifier. The differential signal 720 in the figure is amplified by the amplifier 710 in one preferred embodiment of the present invention, an amplified differential signal 730 is obtained ~~amplified~~.

[0029] The signal amplifier in the foregoing second preferred embodiment is implemented in FIG. 8. The current source 810 and current source 820 supply the currents ~~that is~~ required by signal amplifier. The second terminals of the resistors 870 and 880 are coupled to the ground voltage respectively. The first terminals of the sensor switches 830 and 840 are coupled to the current source 810, the first terminals of the sensor switches 850 and 860 are coupled to the current source 820, the second

terminals of the sensor switches 830 and 850 are coupled to the first terminal of the resistor 870 where the signal 834 is drawn, and the second terminals of the sensor switches 840 and 860 are coupled to the first terminal of the resistor 880 where the signal 832 is drawn. The signal 834 and 832 form[[make]] the differential signal that is transmitted by the signal amplifier. Wherein, if the primitive signal after transient is to be ~~converted and~~ amplified partially in its [[for]] front part[[end]], the sensor switches 830 and 850 are turned on whereas the sensor switches 840 and 860 are turned off. For non-partial amplification, sensor switches 830 and 860 are turned on whereas sensor switches 840 and 850 are turned off.

[0030] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.

ABSTRACT OF THE DISCLOSURE

A cascade driving circuit for a liquid crystal display, including a plurality of driving circuit units, a plurality of differential signal transmitters and a plurality of differential signal receivers. Each of the driving circuit units is disposed with one of the differential signal transmitter, so as to generate a differential signal and propagate which to next stage for each driving circuit unit. Each of the driving circuit units is further disposed with one of the differential signal receivers, so as to receive the differential signal from the previous stage of the driving circuit unit. Therefore, power consumption is reduced with usage of differential signals.